REMARKS

Claims 1, 3-5, 8-12, 14-18 and 20-28 are pending in the present application, were examined, and stand rejected. In response, Claims 6, 9, 12, 15, 18 and 23 are amended, Claim 10 is cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1, 3-6, 8, 9, 11, 12, 14-18 and 20-28 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claims 1, 3-6, 8-12, 14-18, 20-23 and 27-28 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,991,197 issued to Ogura et al. ("Ogura"). Applicants respectfully traverse this rejection.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik v. American Hoist & Derrick* ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)*(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. *Titanium Metals Corp. of American v. Banner* ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

Regarding Claim 1, Claim 1 recites the following features, which are not disclosed by Ogura or the references of record:

> a revision identification register to store a revision identification value of the apparatus, and
>
> a revision identification modification register, the revision identification modification register to allow modification of the revision identification register contents when indicated by the contents of the revision identification modification register. (Emphasis added.)

Conversely, Ogura teaches:

> a nonvolatile semiconductor memory device according to a first embodiment of the present invention. This nonvolatile semiconductor memory device of FIG. 1 is, for example, a flash memory, and includes a memory array 1. Memory array 1 includes a plurality of nonvolatile memory cells arranged in a matrix. (col. 5, lines 59-65.) (Emphasis added.)

As further described by Ogura :

> In memory blocks 1*b* and 1*c* of parameter block region 1*pr*, numeric parameter data that is not so frequently rewritten such as the identification number (ID number) of the memory device, a specific personal user identification number (password number) in the application of an IC card, the telephone number in application of a telephone are stored. In memory blocks 1*d*-1*n* of main block region 1*mr*, data that can be rewritten by the user during general usage is stored. (col. 5, lines 30-38.) (Emphasis added.)

Based on the cited passage above, memory array 1, as taught by Ogura, fails to include either a revision identification register or a revision identification modification register, the contents of which determine whether the revision identification register is enabled to allow modification thereof. Ogura discloses that:

> The nonvolatile semiconductor memory device of the first embodiment further includes a protect control data storage region 2 provided corresponding to respective memory blocks 1*a*-1*n* for storing the value of lock bit LB that controls the inhibition/permission of writing and erasing of memory blocks 1*a*-1*n*. Protect control data storage region 2 includes lock bit storage units 2*a*-2*n* for storing lock bits LBa-LBn in a nonvolatile manner for memory blocks 1*a*-1*n*, respective. (col. 6, lines 12-20.) (Emphasis added.)

Applicants respectfully submit that memory blocks 1*a*-1*n*, as taught by Ogura fail to disclose or suggest a register including a revision identification value of an apparatus, as recited by Claim 1. As a result, the Examiner is prohibited from establishing the disclosure of the revision identification modification register to allow modification of a revision identification value within the revision identification register, as recited by Claim 1 with Ogura as an anticipatory reference.

As known to those skilled in the art, the Peripheral Component Interconnect Local Bus Specification, Rev. 2.2, released December 18, 1998, added a subsystem vendor ID register and a subsystem ID register to the configuration registers provided by a PCI device. As indicated by the PCI Bus Specification Rev. 2.2, the configuration registers include a revision identification register that generally stores an 8-bit revision identification value assigned by a device manufacturer to indicate a revision number of a device.

Applicants respectfully submit that memory blocks 1*a*-1*n* of memory array 1, as taught by Ogura, does not store a revision identification value and therefore fails to teach a revision identification register, as required by the PCI Bus Specification Rev. 2.2 or a revision identification modification register, as recited by Claim 1. Moreover, as disclosed by Ogura:

> The nonvolatile semiconductor memory device of FIG. 1 is, for example, a flash memory, and includes a memory array 1. (col. 5, lines 61-63.) (Emphasis added.)

As indicated by the attached *WEBOPEDIA* definition, a flash memory is a special type of memory that can be erased and reprogrammed and blocked instead of one byte at a time. As indicated by the attached definition, flash memory is often used as BIOS memory.

Conversely, Claim 1 recites registers, and specifically, a revision identification register and a revision identification modification register. As indicated by the attached definition, a register refers to an architectural feature, such as, for example, a high speed storage area within a CPU. As indicated by the attached definition, the number of registers that a CPU has and the size of each (number of bits) help determine the power and speed of a CPU.

Applicants respectfully submit that semiconductor memory devices, such as flash memory, as disclosed in Ogura, refer to components that may be added on to a computer architecture to provide data storage. Conversely, the registers within an architecture may not be expanded by adding on additional components and are often a limitation of legacy computer systems, which include very few architectural registers. Hence, Applicants respectfully submit that a semiconductor memory device, as disclosed in Ogura, does not disclose a register, as recited by Claim 1.

However, the case law establishes that each and every element of a claim must be exactly disclosed in an anticipatory reference to establish a *prima facie* case of anticipation. Id. Here, Applicants respectfully submit that Ogura is not a proper anticipatory reference under §102(b), since the memory blocks 1*a*-1*n* of memory array 1, or the semi-conductor device, as taught by Ogura (*See*, FIG. 1 and col. 5, lines 59-65) fails to disclose a revision identification register having a revision identification modification register associated with the revision identification register to allow modification of a value within the revision identification register, as recited by Claim 1. In other words, the nonvolatile cells semiconductor memory device disclosed in Ogura does not disclose a register as recited by Claim 1.

Consequently, Applicants respectfully submit that the Examiner is prohibited from establishing a *prima facie* case of anticipation of Claim 1 under §102(b) with Ogura as an anticipatory reference to establish a *prima facie* case of anticipation. Lindemann, supra. Therefore, Applicants respectfully submit that Claim 1 is patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 1.

Regarding Claims 6 and 12, Claims 6 and 12 are amended to recite the following claim feature, which is neither disclosed nor suggested by Ogura:

> replacing the current revision identification value with a revision identification value that indicates the first device stepping if the current revision identification value does not indicate the first device stepping. (Emphasis added.)

As defined in Applicants' specification:

> This first device stepping may be the last stepping where any significant changes in functionality occurred. The term "first device stepping" does not necessarily mean the original version of a device or functional unit. (pg. 7, ¶[0022], lines 5-8.) (Emphasis added.)

Accordingly, based on the cited passage above, Applicants' specification defines the term "first device stepping" to refer to a previous device stepping whereas the term "updated device stepping" refers to a device stepping referring to a new revision to provide a new device stepping. As indicated by the PCI Bus Specification Rev. 2.2, the configuration registers include a revision identification register that generally stores an 8-bit revision identification value assigned by a device manufacturer to indicate a revision number of a device.

Conversely, as disclosed in Ogura:

> In memory blocks 1*b* and 1*c* of parameter block region 1*pr*, numeric parameter data that is not so frequently rewritten such as the identified number (ID number) of the memory device, a specific personal user identification number (password number) in the application of an IC card, the telephone number in application of a telephone are stored. (col. 6, lines 12-17.) (Emphasis added.)

Assuming, arguendo, that the identification number, or ID number, of the memory device disclosed a device stepping of the memory device, according to the Examiner, Ogura teaches determining whether to modify a value stored in a revision identification register at col. 7, lines 1-8. (*See*, pg. 2, ¶4 of Office Action mailed June 14, 2005.) As disclosed by Ogura:

> In status register 9, a register is provided for storing status data indicating whether data is programmed properly with respect to a memory cell in data writing and data indicating whether data is properly erased in an erasure operation. LB read/write circuit 8 carries out writing/reading with respect to a corresponding lock bit according to a lock address signal (not explicitly shown) when rewrite of a lock bit is specified under control of control circuit 4. (col. 7, lines 1-8.) (Emphasis added.)

Assuming, arguendo, that Ogura teaches determining whether to modify a value stored in the revision identification register, Ogura fails to disclose that the current revision identification value is replaced with a revision identification value that indicates a first device stepping if the current revision identification value indicates an updated device stepping. as recited by amended Claims 6 and 12. Although Ogura teaches techniques for determining whether to unlock/lock the lock bit of a lock bit storage unit 2*a*-2*n* lock bit, for example, as shown in the flowchart of FIG. 10, Ogura is devoid of and hence, fails to disclose the replacing of an updated device stepping with a first device stepping, as recited by amended Claims 6 and 12, which as defined by Applicants' specification refers to the last device stepping where any significant changes in functionality occurred. (*See*, pg. 7, ¶[0022], lines 5-7.)

Hence, Applicants respectfully submit that the disclosure in Ogura to provide a lock bit for protecting, for example, memory block 1*c* and 1*b*, which refer to parameter blocks, which may store, for example, an identification number (ID number) of the memory device (*see*, col. 6, line 15) and the locking of such data based on lock bits 2*b* and 2*c*, as shown in FIG. 1, fail to teach the replacing of an updated identification number with a previous identification number, for example, as required to anticipate the features required by Claims 6 and 12. (*See*, col. 6, lines 30-38.)

Accordingly, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of anticipation due to the failure to illustrate the presence in the single prior art reference disclosure of each and every element recited by amended Claims 6 and 12, as arranged in the respective claims. Lindemann, supra. Accordingly, Applicants respectfully submit that the Examiner is prohibited from relying on Ogura as an anticipatory reference to anticipate the above-recited features of amended Claims 6 and 12, since Ogura fails to exactly disclose each and every

element recited by amended Claims 6 and 12, and specifically, replacing of an updated device stepping with a first or previous device stepping, as recited by amended Claims 6 and 12. Banner Titanium, supra.

Accordingly, amended Claims 6 and 12 are patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 6 and 12.

Regarding Claims 8-11, Claims 8-11, based on their dependency from Claim 6, are also patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 8-11.

Regarding Claim 14, Claim 14, based on its dependency from Claim 12, is also patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 14.

Regarding Claims 9 and 15, Claims 9 and 15 are amended to recite the following claim feature, which is neither disclosed nor suggested by either Ogura or the references of record:

> executing a pre-operating system software agent, the pre-operating software agent to determine whether a value stored in a revision identification register indicates a first device stepping;
>
> accessing a revision identification modification register;
>
> modifying the value stored in the revision identification register to indicate the first device stepping if modification of the revision identification register is enabled according to contents of the revision identification modification register and the value stored in the revision identification register indicates an updated device stepping. (Emphasis added.)

For at least the reasons indicated above regarding the rejection of Claims 6 and 12, Applicants respectfully submit that the above-described arguments provided with regards to the rejection of Claims 6 and 12 are applicable to the Examiner's rejection of Claims 9 and 15 under 35 U.S.C. §102(b). Specifically, although Ogura discloses the storage of an identification, or ID, number of a memory device (*see*, col. 6, line 15), Ogura fails to disclose that such identification, or ID, number is modified to indicate a first or previous device stepping if modification of the revision identification register is enabled according to the contents of the revision identification modification register and the value stored in the revision identification register indicates a new or updated device stepping, as recited by Claims 9 and 15. In other words, the disclosure in Ogura, for determining whether to lock or unlock lock bit storage units 2*a*-2*n* is associated with the various memory blocks 1*a*-1*n* of memory array 1 shown in FIG. 1 of Ogura, fails to disclose or suggest the modifying of an updated device stepping with a first device stepping when enabled according to a revision identification modification register, as recited by Claims 9 and 15.

Accordingly, Applicants respectfully submit that the Examiner fails to illustrate the presence in a single prior art reference disclosure of each and every element recited by Claims 9 and 15, as

arranged in the respective claims, as required to establish a *prima facie* case of obviousness. Lindemann, supra. Accordingly, Applicants respectfully submit that the Examiner is prohibited from establishing a *prima facie* case of anticipation of Claims 9 and 15 with Ogura as an anticipatory reference, since Ogura fails to exactly disclose each and every element recited by amended Claims 9 and 15. Banner Titanium, supra.

Accordingly, Claims 9 and 15 are patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 9 and 15.

Regarding Claim 11, Claim 11, based on its dependency from Claim 9, is also patentable Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 11.

Regarding Claims 16 and 17, Claims 16 and 17, based on their dependency from Claim 15, are also patentable Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 16 and 17.

Regarding Claim 18, Claim 18 is amended to recite the following claim features, which are neither disclosed nor suggested by Ogura or the references of record:

> at least one functional unit coupled via a communications link with a device, the functional unit including:
>
> a revision identification register to store a revision identification value of the device; and
>
> a revision identification modification register, the revision identification modification register to allow modification of the revision identification register contents when indicated by the contents of the revision identification modification register; and
>
> a non-volatile memory to store a pre-operating system software agent, the pre-operating software agent to determine whether to modify an updated device stepping stored in the revision identification register with a first device stepping. (Emphasis added.)

In contrast to the above-recited features of amended Claim 18, Ogura teaches a non-volatile semiconductor memory device, for example, as shown in FIG. 1. As disclosed in Ogura:

> Memory array 1 includes a plurality of nonvolatile memory cells arranged in a matrix. Memory array 1 is divided into a plurality of memory blocks 1*a*-1*n*. Each memory block includes a plurality of memory cells arranged in a matrix. These memory blocks 1*a*-1*n* are divided into a boot block region 1*br*, a parameter block region 1*br*, and a main block region 1*mr* according to the attribute of the stored data, Memory block 1*a* is used as the boot block. Memory blocks 1*b* and 1*c* are used as the parameter block. Memory blocks 1*d*-1*n* are used as the main block. (col. 5, line 63 - col. 6, line 6.) (Emphasis added.)

As further recited by Ogura:

> The nonvolatile semiconductor memory device of the first embodiment further includes a protect control data storage region 2 provided corresponding to

> respective memory blocks 1*a*-1*n* for storing the value of lock bit LB that controls the inhibition/permission of writing and erasing of memory blocks 1*a*-1*n*. Protect control data storage region 2 includes lock bit storage units 2*a*-2*n* for storing lock bits LBa-LBn in a nonvolatile manner for memory blocks 1*a*-1*n*, respectively. (col. 6, lines 30-38.) (Emphasis added.)

Based on the cited passages above, the non-volatile semiconductor memory device, as disclosed in Ogura, includes protect control data storage region 2 integrated with memory array 1. Conversely, Claim 18, as amended, recites at least one functional unit coupled via a communications link with a device. As further recited by Claim 18, this functional unit includes a revision identification register and a revision identification modification register. Accordingly, as recited by amended Claim 18, this functional unit is separate from a device, such as, for example, the semiconductor memory device as disclosed in Ogura.

Hence, Applicants respectfully submit that Ogura fails to disclose at least one functional unit, which includes a revision identification register and a revision identification modification register separate from a device, such as the semiconductor memory device disclosed in Ogura. In other words, Ogura teaches that the memory array 1 and protect control data storage region 2 are integrated within the device, in contrast to the above-recited features of amended Claim 18. (*See*, supra.)

Furthermore, as recited by amended Claim 18:

> a non-volatile memory to store a pre-operating system software agent, the pre-operating software agent to determine whether to modify an updated device stepping stored in the revision identification register with a first device stepping. (Emphasis added.)

For at least the reasons indicated above with regard to the rejection of independent Claims 9 and 15, the disclosure in Ogura is directed to providing techniques for determining whether to lock or unlock lock bits 2*a*-2*n* of protect control data storage region 2, for example, as shown in FIG. 10. Accordingly, Applicants respectfully submit that the Examiner fails to illustrate the presence in a single prior art reference disclosure of each and every element recited by amended Claim 18, as arranged in Claim 18, as required to establish a *prima facie* case of obviousness. Lindemann, supra. Accordingly, Applicants respectfully submit that the Examiner is prohibited from establishing a *prima facie* case of anticipation with Ogura as an anticipatory reference since Ogura fails to exactly disclose each and every element recited by amended Claim 18. Banner Titanium, supra.

Accordingly, amended Claim 18 is patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 18.

Regarding Claims 20-22, Claims 20-22, based on their dependency from Claim 18, are also patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 20-22.

Regarding Claim 23, Claim 23 is amended to recite the following claim feature, which is neither disclosed nor suggested by Ogura or the references of record:

> at least one functional unit coupled via a communications link with a device, the functional unit including:
>
> a revision identification register to store a revision identification value of the device, and
>
> a revision identification modification register, the revision identification modification register to allow modification of the revision identification register contents when indicated by the contents of the revision identification modification register to restore the revision identification value of the device. (Emphasis added.)

For at least the reasons indicated above with reference to the rejection of Claim 18, Ogura fails to disclose a functional unit coupled via a communications link with a device where the functional unit includes a revision identification register and a revision identification modification register. Assuming, arguendo, that Ogura teaches a revision identification and a revision identification modification register, such registers are incorporated within the device or semiconductor memory taught by Ogura and are, therefore, not incorporated within a functional unit coupled to, for example, the memory device taught by Ogura, via a communications link, as recited by amended Claim 23. (*See*, col. 5, line 63 - col. 6, line 6 and col. 6, lines 30-38.)

Furthermore, for at least the reasons indicated above with regards to the rejections of Claims 6 and 12, the revision identification modification register, as recited by Claim 23, dictates whether to restore a revision identification value of the device. In contrast to restoring a revision identification value of a device, the disclosure in Ogura is directed to techniques for determining whether to lock or unlock locked bits of protect control data storage region 2 and therefore, fails to disclose or suggest the restoring of a revision identification value of a device according to the contents of a revision identification modification register, as recited by Claim 23.

Accordingly, Applicants respectfully submit that the Examiner fails to illustrate the presence in a single prior art reference disclosure of each and every element recited by amended Claim 23, as arranged in amended Claim 23, as required to establish a *prima facie* case of obviousness. Lindemann, supra. Therefore, Applicants respectfully submit that the Examiner is prohibited from establishing a *prima facie* case of anticipation with Ogura as an anticipatory reference, since Ogura fails to exactly disclose each and every element recited by amended Claim 23. Banner Titanium, supra.

Accordingly, Claim 23, as amended, is patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 23.

Regarding Claim 27, Claim 27 recites the following claim feature, which is neither disclosed nor suggested by either Ogura or the references of record:

> restoring the value within the revision identification register to indicate a first device stepping if the revision identification modification register contents indicate that the revision identification register will accept writes. (Emphasis added.)

For at least the reasons provided above, Applicants respectfully submit that the disclosure in Ogura is limited to a semiconductor memory including a memory array 1, which includes a plurality of memory blocks 1*a*-1*n* coupled to a protect control data storage region 2, which includes a plurality of lock bits 2*a*-2*n*. Applicants respectfully submit that the disclosure in Ogura, for example, as illustrated with reference to FIG. 10, is directed to techniques for determining whether to lock or unlock lock bits 2*a*-2*n* of protect control data storage region 2. Hence, Applicants respectfully submit that Ogura fails to disclose the restoring of a revision identification register to indicate a first device stepping according to the contents of a revision identification modification register, as recited by Claim 27.

Consequently, Applicants respectfully submit that the Examiner fails to illustrate the presence in a single prior art reference disclosure of each and every element recited by Claim 27, as arranged in Claim 27, as required to establish a *prima facie* case of obviousness. Lindemann, supra. Hence, Applicants respectfully submit that the Examiner is prohibited from establishing a *prima facie* case of anticipation with Ogura as an anticipatory reference, since Ogura fails to exactly disclose each and every recited feature of Claim 27. Banner Titanium, supra.

Accordingly, Applicants respectfully submit that Clam 27 is patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 27.

Regarding Claim 28, Claim 28 recites a bus device comprising:

> a plurality of configuration registers, the plurality of configuration registers including a revision identification register to store a revision identification value of the bus device, and a revision identification modification register, the revision identification modification register to allow modification of the revision identification register contents when indicated by contents of the revision identification modification register. (Emphasis added.)

In contrast to disclosing a bus device, as recited by Claim 27, Ogura discloses a semiconductor memory device, which includes a memory array comprising memory blocks 1*a*-1*n* and a protect control data storage region 2 comprising a plurality of lock bits 2*a*-2*n*. (*See*, col. 5, line 63 - col. 6, line 6, and col. 6, lines 30-38.) As indicated by Ogura:

> This nonvolatile semiconductor memory device of FIG. 1 is, for example, a flash memory, and includes a memory array 1. (col. 5, lines 61-63.)

Applicants respectfully submit that the semiconductor memory device disclosed by Ogura fails to disclose or suggest a bus device, as recited by Claim 27. Furthermore, Claim 27 recites a plurality of configuration registers including a revision identification register and a revision identification modification register. Applicants respectfully submit that the memory blocks of memory array 2, as shown in FIG. 1 of Ogura, as well as lock bits 2*a*-2*n* of protect control data storage region 2, do not disclose configuration registers, as recited by Claim 28.

Therefore, Applicants respectfully submit that the Examiner fails to illustrate the presence in a single prior art reference disclosure of each and every element recited by Claim 28, as arranged in Claim 28, as required to establish a *prima facie* case of anticipation. Lindemann, supra. Accordingly, Applicants respectfully submit that the Examiner is prohibited from establishing a *prima facie* case of anticipation with Ogura as an anticipatory reference, since Ogura fails to exactly disclose each and every element recited by amended Claim 28. Banner Titanium, supra.

Accordingly, Claim 28 is patentable over Ogura, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 28,

II. Claim Rejections Under 35 U.S.C. §103

The Examiner rejects Claims 24-26 under 35 U.S.C. §103(a) as being unpatentable over Ogura. Applicants respectfully traverse this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art references must teach or suggest all the claim limitations. [MPEP §2142] Based on Applicants' arguments provided below, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Regarding the Examiner's rejection of Claims 24-26 under 35 U.S.C. §103(a), Applicants respectfully submit that the Examiner's rejection fails to rectify the deficiencies of Ogura in teaching at least one functional unit, which includes a revision identification register and a revision modification register coupled via a communications link with a device, as recited by Claim 23.

Applicants respectfully submit that assuming, arguendo, that Ogura teaches a revision identification register and a revision modification register, Applicants respectfully submit that such teachings integrate such registers within the semiconductor memory device, as disclosed in Ogura. In other words, the memory array 1 of semiconductor memory including memory blocks 1*a*-1*n*, which are coupled to and integrated with protect control data storage region 2 to include lock bits

2*a*-2*n*, are integrated within the semiconductor memory device and are, therefore, not incorporated within a functional unit, which is coupled to the semiconductor memory device via communications link, as recited by amended Claim 23.

Accordingly, Applicants respectfully submit that amended Claim 23 is patentable over the combination of Ogura, as well as the skill in the art. Consequently, Claims 24–26, based on their dependency from Claim 23, are also patentable over the combination of Ogura and the skill in the art. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 24-26.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1, 3-6, 8, 9, 11, 12, 14-18 and 20-28, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: August 29, 2005

By: _____
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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 29, 2005

_____
Marilyn Bass August 29, 2005

Exhibit 1: *WEBOPEDIA* definitions of "flash memory" and "register"